IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 3, 6-9, and 11 in accordance with the following:

1. (CURRENTLY AMENDED) An apparatus for branch prediction, comprising:

a history register ~~which stores therein~~storing history of previous branch instructions;

an index generation circuit ~~which generates~~generating a first index from an instruction address and the history stored in said history register;

a history table ~~which stores therein~~storing a tag, which is a portion of the instruction address, ~~as a tag~~ and a first count value indicative of a likelihood of branching in association with the first index;

a branch destination buffer ~~which stores therein~~storing a branch destination address or a predicted branch destination address of an instruction indicated by the instruction address and a second value indicative of a likelihood of branching in association with a second index that is at least a portion of the instruction address; and

a selection unit ~~which makes~~making a branch prediction by selecting one of the first value and the second value.

2. (ORIGINAL) The apparatus as claimed in claim 1, wherein said selection unit selects the first value if said branch destination buffer has an entry therein corresponding to a current instruction address and said history table has an entry therein corresponding to the current instruction address and current history, and selects the second value if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history.

3. (CURRENTLY AMENDED) The apparatus as claimed in claim 2, wherein said selection unit ~~predicts~~ makes the branch prediction indicating no branching if said branch destination buffer does not have an entry therein corresponding to the current instruction address.

4. (ORIGINAL) The apparatus as claimed in claim 1, wherein said index generation circuit generates the first index that is an Exclusive-OR between the history stored in said history register and the current instruction address.

5. (ORIGINAL) The apparatus as claimed in claim 1, wherein more than one said history table is provided so as to allow a plurality of entries to be registered with respect to said first index.

6. (CURRENTLY AMENDED) A processor, comprising:

a history register ~~which stores therein~~storing history of previous branch instructions;

an index generation circuit ~~which generates~~generating a first index from an instruction address and the history stored in said history register;

a history table ~~which stores therein~~storing a tag, which is a portion of the instruction address, ~~as a tag~~ and a first count value indicative of a likelihood of branching in association with the first index;

a branch destination buffer ~~which stores therein~~storing a branch destination address of an instruction indicated by the instruction address and a second value indicative of a likelihood of branching in association with a second index that is at least a portion of the instruction address;

a selection unit ~~which makes~~making a branch prediction by selecting one of the first value and the second value;

an execution control unit ~~which controls~~controlling execution of instructions; and

an execution operation unit ~~which executes~~executing the instructions.

7. (CURRENTLY AMENDED) A method of branch prediction, comprising ~~the steps of~~:

~~providing a history table which stores therein~~ storing a tag, which is a portion of an instruction address, ~~as a tag~~ and a first count value indicative of a likelihood of branching in association with a first index that is generated from the instruction address and history of a ~~pervious~~ previous branch instruction[[s]];

~~providing a branch destination buffer which stores therein~~storing a branch destination address in a branch destination buffer of an instruction indicated by the instruction address and a second value indicative of a likelihood of branching in association with a second index that is

at least a portion of the instruction address selecting one of a first value and a second value; and

predicting branching in response to the selected one of the first value and the second value.

8. (CURRENTLY AMENDED) The method as claimed in claim 7, wherein said ~~step of~~ selecting one of the first value and the second value selects the first value if said branch destination buffer has an entry therein corresponding to a current instruction address and said history table has an entry therein corresponding to the current instruction address and current history, and selects the second value if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history.

9. (CURRENTLY AMENDED) The method as claimed in claim 8, further comprising ~~the steps of~~:

registering the current instruction address in said branch destination buffer if said branch destination buffer does not have an entry therein corresponding to the current instruction address; and

registering information about the current instruction address in the history table if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history and if a prediction made based on the second value turns out to be erroneous.

10. (ORIGINAL) The method as claimed in claim 9, wherein the information about the current instruction address is not registered in said history table if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history and if the prediction made based on the second value turns out to be correct.

11. (CURRENTLY AMENDED) An apparatus for branch prediction, comprising:

a history register ~~which stores therein~~storing history of immediately preceding branch instructions;

an index generation circuit ~~which generates~~generating a first index that is an Exclusive-OR between an instruction address and the history stored in said history register;

a history table ~~which stores therein~~storing a tag, which is a portion of the instruction address, ~~as a tag~~ and a first count value indicative of a likelihood of branching in association with ~~each~~ said first index;

a branch destination buffer ~~which stores therein~~storing ~~a~~ the portion of the instruction address as ~~a~~ the tag, a branch destination address of an instruction indicated by the instruction address, and a second value indicative of a likelihood of branching in association with said ~~each~~ second index that is a portion of the instruction address; and

a selection unit ~~which makes~~making a branch prediction by selecting one of the first value and the second value, wherein said selection unit selects the first value if said branch destination buffer has an entry therein corresponding to a current instruction address and said history table has an entry therein corresponding to the current instruction address and current history, and selects the second value if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history.

12. (NEW) A method for predicting branching of an instruction, comprising:

correlating a tag representing a part of a branch instruction address for the instruction with a count value indicative of a likelihood of branching occurring; and

comparing said tag with an index to assist in determining whether branching should occur based on said count value.

13. (NEW) An apparatus for predicting branching of an instruction, comprising:

an XOR circuit adapted to perform an XOR operation on a portion of a branch instruction address and contents of a history register to generate an index;

a comparison unit adapted to compare said index with a tag representing a portion of an instruction address; and

a selection unit adapted to perform a count value selection based on said comparison to determine branching of said instruction.

14. (NEW) A method for predicting branching of an instruction, comprising:

providing a correlation in which a tag representing a part of a branch instruction address is correlated with a first count value;

providing a correlation in which a tag is correlated with a second value; and

selecting one of said first count value and said second value to predict branching of said instruction depending upon whether an index is matched to said tag in said first correlation or said tag in said second correlation.